Software Stacks for Mixed-critical Applications: Consolidating IEEE 802.1 AVB and Time-triggered Ethernet in Next-generation Automotive Electronics

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***Abstract*—Real-time Ethernet variants are expected to build the future communication infrastructure in cars. First camera based driver assistance functions will communicate using IEEE 802.1 AVBs credit-based shaping. But for the strict timing requirements of automotive control-traffic, AVBs current timing guarantees are insufficient. The upcoming IEEE 802.1Qbv standard proposes synchronous time-triggered traffic to overcome these limitations. This paper presents a low footprint microcontroller based communication architecture, that supports both traffic classes in parallel while using standard hardware components. It allows first realistic performance analyses of coexistent traffic shaping strategies in a software based implementation.**

I. Introduction

Today's automobiles utilise an increasing number of electronic control units (ECUs) to implement the various safety and comfort functions offered in recent cars. For each application a set of ECUs, physically distributed over the whole vehicle, is required. This architecture demands a communication infrastructure that is able to transport data with high predictability and exact timing. For legacy reasons, several different communication technologies, each optimised for specific use-cases, are used today. Examples are the Controller Area Network (CAN) [1], Media Oriented Systems Transport (MOST) [2] or FlexRay [3]. This technology diversity led to a highly heterogeneous in-car network that is extremely complex, difficult to develop, configure and maintain, and in terms of bandwidth consumption at its limits.

Real-time Ethernet is a promising solution to reduce the complexity imposed by today's heterogenous, gateway-based automotive networks, while providing additional bandwidth for upcoming features. Ethernet will enter the automobile through in-car multimedia and camera based driver assistance systems with moderate timing guarantees in the range of microseconds, which is a typical use-case for the Ethernet Audio/Video Bridging (AVB) protocol suite [4]. This first generation uses Ethernet as an additional communication infrastructure, which runs in parallel to the well-established communication technologies (e.g. CAN, FlexRay, MOST, ...) and provides the bandwidth required by new driver assistance functions, for example camera based advanced driver assistance systems (ADAS).

The second generation of switched real-time Ethernet based communication structures in cars will provide a backbone for a subset of applications of different in-car domains. While in this architecture some ECUs will be equipped with an Ethernet interface, other ECUs will still be connected with the backbone via a CAN to Ethernet gateway. Some of the applications that will be transferred to Ethernet in the second generation require a latency below 1 ms over up to seven hops. These rigid real-time requirements cannot be achieved with today's AVB protocol suite. Recently, the standardisation of scheduled traffic was started to improve AVB to satisfy the requirements of ultra low latency and jitter [5]. IEEE 802.1Qbv (Enhancements for Scheduled Traffic) adds synchronous time-triggered messages to the event-based shaping of AVB. This traffic is based on a coordinated time-division multiple access (TDMA) scheme and prevents concurrent access of outgoing line cards to achieve a deterministic transmission.

The concurrent utilisation of the same physical Ethernet by different traffic classes, like AVB, time-triggered, and standard best-effort traffic, causes effects of interference that have to be carefully regarded when designing automotive networks. To evaluate the concepts of Ethernet AVB with additional time-triggered scheduling, we contribute a prototype architecture and implementation of the traffic shaping concepts in a software stack for an ARM9 based system-on-chip. Using this architecture, first design concepts for in-car networks with upcoming standards such as IEEE 802.1Qbv [5] can be evaluated on a hardware platform that is based on standard components and offers realistic performance and temporal characteristics, comparable with certified automotive hardware. The focus of this work is to provide a prototype platform for various use-cases. For example, gateways between real-time Ethernet and legacy fieldbuses that require a variety of different service classes.

This paper is organised as follows: In Section II, we introduce the concepts of Ethernet AVB and time-triggered Ethernet and present previous and related work. Section III presents the concept and architecture. In Section IV, details from the implementation as well as the evaluation results are shown and discussed. Finally, Section V concludes our work and gives an outlook on our future research.

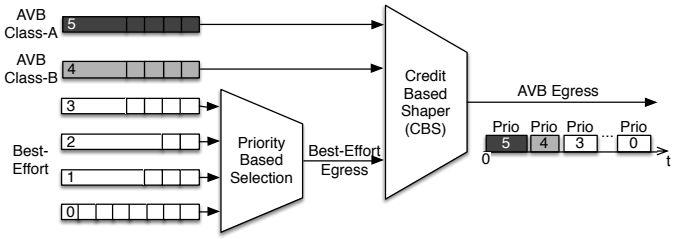

Fig. 1. IEEE 802.1Qav Sender/Forwarding: Transmission selection scheme

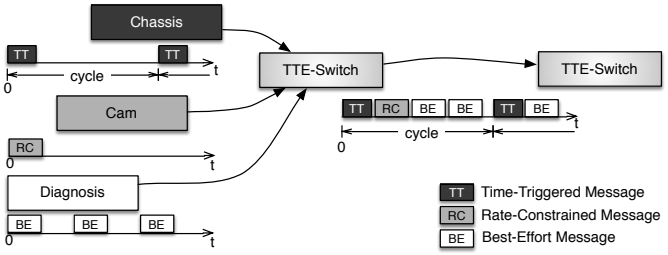

Fig. 2. Prioritising and time-triggered media access in time-triggered Ethernet

II. Background & Related Work

A. IEEE 802.1 AVB

The IEEE 802.1 Audio/Video Bridging (AVB) [4] suite consists of protocols for low latency streaming over 802 networks. Besides extensions for network management, it defines precise *time synchronisation* (IEEE 802.1QAS) with a synchronisation error of less than $1\,\mu s$ over a maximum of seven hops [6], [7], dynamic *stream reservation* (IEEE 802.1Qat) and real-time *traffic shaping* (IEEE 802.1Qav) for time sensitive applications.

IEEE 802.1Qav defines queuing and forwarding rules for real-time streams using strict priorities and credit based shaping (CBS). For latency requirements up to a maximum of $2\,ms$ over seven hops, stream reservation (SR) class-A was defined. SR class-B guarantees latency requirements of up to $50\,ms$. All other traffic is treated as best-effort traffic using legacy Ethernet frames. Transmission selection and traffic shaping in IEEE 802.1Qav uses a credit based shaping (CBS) algorithm with priorities. The transmission of a SR class frame is only allowed when the amount of available credits is greater or equal 0. An upper and lower bound of the credit based shaper limits the streams bandwidth and burstiness. Figure 1 shows the scheme for transmission selection.

To realise a dynamic online registration of new real-time streams, Ethernet AVB defines the IEEE 802.1Qat [8] Stream Reservation Protocol (SRP). It provides a three step signalling process (i.e., stream advertisement, registration and deregistration) to reserve the required resources along the path between sender and receiver.

B. Time-triggered Ethernet

Besides several other real-time extensions for standard Ethernet, e.g. PROFINET [9], TTEthernet (AS6802) [10] is a time-triggered extension for Ethernet based communication with low latency and jitter. AS6802 is standardized by the Society of Automotive Engineers (SAE) [11]. It features three different traffic classes:

For *time-triggered* (TT) communication, pre-configured schedules assign dedicated transmission slots to each participant. This *coordinated* time-division-multiple-access (TDMA) multiplexing strategy allows deterministic transmission with predictable delay. It prevents congestion on outgoing line cards and enables isochronous communication with low latency and jitter. To realise the TDMA concept, a failsafe synchronisation protocol, with an error below $1\,\mu s$, implements a global time among all participants.

In addition to synchronised time-triggered messages, two event-triggered message classes are defined: *Rate-constrained* (RC) traffic is intended for the transmission of messages with moderate timing requirements. It limits the streams bandwidth and prioritises according to the strategy of the *ARINC-664 (AFDX)* protocol [12]. The characteristics of RC traffic are comparable with AVBs SR Classes A and B.

Best-effort (BE) traffic conforms to standard Ethernet messages that are transmitted with the lowest priority. The latter allows the integration of hosts that are unaware of the real-time protocol and remain unsynchronised. These nodes communicate using best-effort messages. Figure 2 shows the media access policy for messages of different traffic classes.

Due to the early state of IEEE 802.1Qbv, in this paper the time-triggered traffic class of AS6802 is used in conjunction with IEEE 802.1Qav [13]. Nevertheless, the nature of time-triggered traffic will allow to transfer the results to an upcoming IEEE standard with scheduled traffic.

C. Related & Previous Work

In previous performance assessments, strengths and weaknesses of time-triggered Ethernet and AVB were revealed and an approach with AVB and time-triggered messages on a shared infrastructure – as contributed in this work – was proposed [14]. There are already microcontroller based AVB software stacks available. XMOS offers an AVB reference design [15] that – in contrast to the concept of this work – relies on a multicore-platform and does not support scheduled traffic. Their xCORE architecture distributes the application and the AVB stack on different processor cores to allow interference free execution of different tasks.

Other strategies than time-triggered messages to improve end-to-end latency in AVB networks are analysed by Imtiaz, Jasperneite and Weber [16]. In place of scheduled traffic, the authors argue in favour of smaller frames to reduce the impact of congestion.

The general feasibility of a software based time-triggered real-time communication stack was shown in previous work [17]. Further, the concept of a credit based shaper (CBS) with support for time-triggered scheduling was previously evaluated using event-based simulation [18].

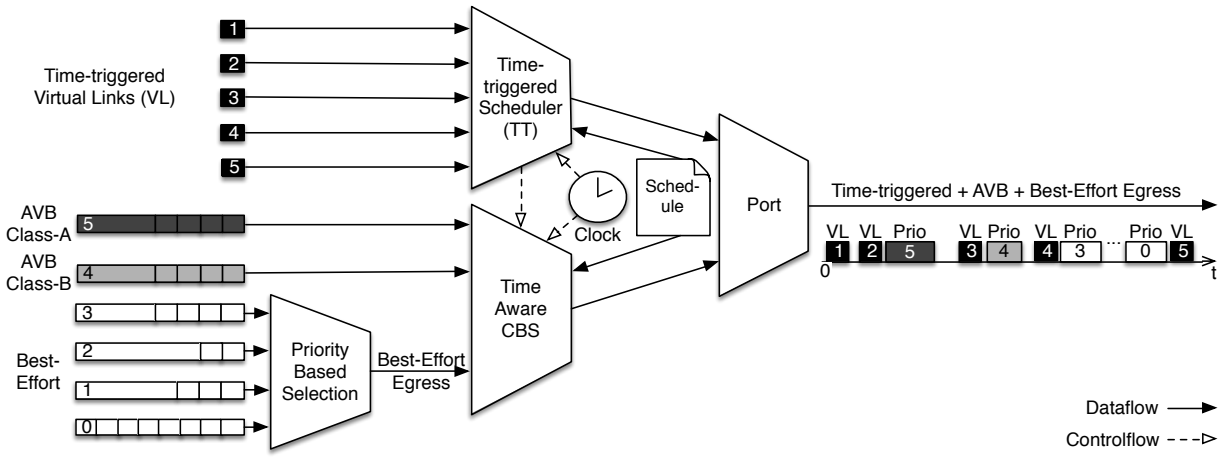

Fig. 3. Transmission Selection Algorithm for AVB and time-triggered traffic. CBS uses clock and schedule, enabling TT communication with no interference

III. Concept & Architecture

A software stack for mixed-critical applications requires reliable timing to schedule message transmission and task execution to ensure that critical applications match their given boundaries. The synchronisation process is important for time-triggered protocols and therefor must be supported by the architecture. Furthermore, the bandwidth of 100 Mbit/s per port demands a memory architecture that is able to manage high data throughput. Due to fault tolerance through redundancy, the system has to handle transmission and reception on multiple ports concurrently.

A. Time Aware Credit Based Shaper

Figure 3 shows our concept for a time aware credit based shaper (CBS) which joins scheduled time-triggered traffic and traffic shaped using the IEEE 802.1Qav algorithms. Time-triggered traffic is not allowed to be delayed by any other frame, though the TT frames must have the highest priority. This requirement conflicts with the service class A of IEEE 802.1Qav that uses the highest priority for its end-to-end performance guarantees. Due to the modified priorities in our concept, changes in the queueing and scheduling strategy of the AVB frames must be made.

In our concept, the time-triggered send-windows and the domain wide synchronised clock are used as input for the Credit Based Shaping (CBS) algorithm (see Figure 3). This allows the algorithm to checks whether a transmission can be finished before the next TT window starts. If no frame fits, the transmitter remains idle until the transmission of the next scheduled TT frame begins. This idle time – sometimes referred to as guard band – guarantees that AVB and best-effort frames will never interfere with TT frames.

The new time aware CBS will introduce further delays for all traffic classes of AVB. For example, if an AVB frame is ready to be transmitted and too large to be sent before the start of the next TT window, the AVB frame will be queued. In previous work we already showed that with a valid schedule the latency guarantee of SR class A (2 ms over 7 hops) is twice as long (4 ms) as in the original standard [18].

B. Partition

An extended scheduler has to be designed to avoid congestion in the mixed-critical applications, using time-triggered Ethernet and AVB. The concept behind this scheduler is to reassign priorities to give time-triggered traffic the highest priority followed by AVB classes A & B and best-effort traffic. Since the time-critical time-triggered slots are static and known before runtime, the scheduler is configured with the time-triggered timing, so that the unused scheduling time can be used to schedule AVB and best-effort traffic (see Figure 3).

C. Architecture

Besides the AVB stack components with the dynamic stream reservation module (IEEE 802.1Qat), there are buffers for each Stream Reservation (SR) class – where class A has the second highest priority, and an interval length of 125 µs and a maximum latency of 2 ms over seven hops – to hold incoming and outgoing frames. Both stacks share the synchronisation module, best-effort modules, and have a scheduler which ensures that there is no frame interference between AVB and time-triggered Ethernet packets. The resulting architecture is shown in Figure 4.

In addition, the architecture uses a dedicated Stream Reservation Protocol (SRP) module that works according to IEEE 802.1Qat [8] to implement an online signalling protocol for the real-time service classes of AVB. This module must work independent from the real-time scheduling and is not allowed to interfere with real-time traffic. Thus the platform must provide strict priorities to prevent interference by the stream reservation frames.

For the communication between the AVB stack and the mixed-critical applications the architecture introduces a dedicated AVB-API that is derived from the implementation of the API of the TTEthernet protocol.

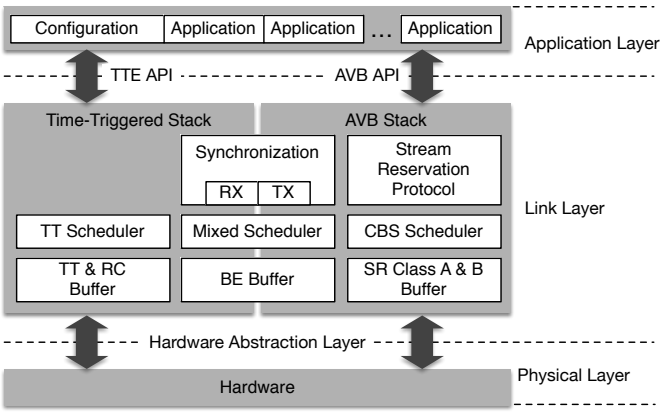

Fig. 4. Mixed critical stack architecture, time-triggered Ethernet and AVB

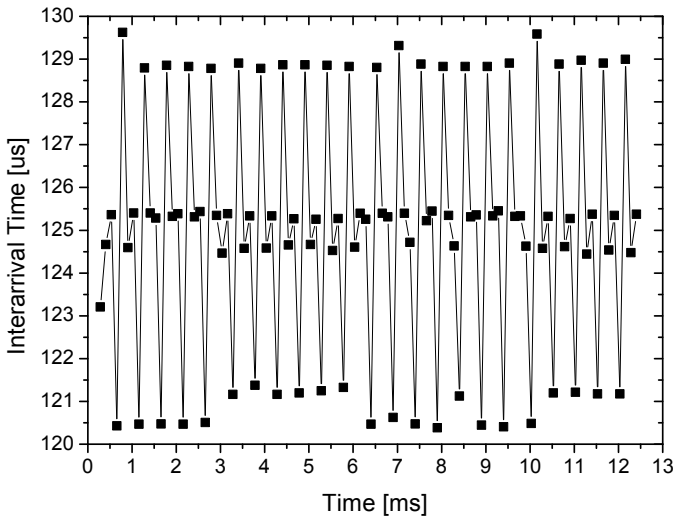

Fig. 5. Interarrival time at the application layer using the presented approach at the sender and receiver side

IV. Implementation & Evaluation Results

A. Platform

The concept is based on a highly integrated hardware platform using a system-on-chip design developed by Hilscher [19]. The modular platform design provides four independently configurable communication channels for various communication technologies like Ethernet or CAN [1] with dedicated Arithmetic Logic Unit (ALU). The ALU is programmable to implement MAC (Medium Access Controller), PEC (Protocol Execution Controller) and, especially for Ethernet, PHY (Physical interface) functionality. The ALUs of all channels operate concurrently.

For the application code and software stacks an ARM926EJ CPU is integrated which runs at 200 MHz. It provides a memory management unit, 8 kB data- and 16 kB instruction cache, 8 kB tightly coupled data memory and a 32 kB ROM holding the boot loader and a real-time kernel. It also provides an internal memory of 144 kB RAM. The data transfer between the communication channels and the CPU is provided by a data switch, which replaces the usual AMBA (Advanced Microcontroller Bus Architecture). This switch is able to open up to five communication channels at the same time and thereby allows to send and receive multiple frames on different ports concurrently.

A dedicated system time module provides timestamps for incoming frames and is used to schedule the time-triggered code execution. It is clocked with 100 MHz and uses an adjustable increment in a resolution of 2^{-28} ns to compensate deviation and drift of the oscillator. This precisely adjustable clock is used to manage and maintain a stable time base for the clock synchronisation.

Comparing the memory consumption of the software stack modules, the TTEthernet part requires 150 kB. The AVB implementation adds 192.1 kB. The consumption of the sub modules is listed in Table I. Since they combine the major functions of AVB, the CBS (29 %), AVB (32.5 %) and MRP (21.8 %) modules are the largest.

B. Evaluation

To quantify the overhead imposed by the stream reservation protocol, CPU utilisation for the periodic update and the processing of incoming MRP frames is measured. The periodic task requires 34.98 µs per update. As it is triggered only once per second it is negligible. The processing of MRP frames adds 3.55 µs to the standard reception routine. As the number of MRP frames correlates to the number of participants, bursts of MRP frames can occur in large networks. In this case the stream reservation may be delayed as the frame processing time exceeds the transmission time. The MRP protocol is based on best-effort traffic and allows these small delays.

Furthermore the quantified overhead imposed by the CBS (Credit Based Shaper) and the accuracy of the inter-arrival times on the sender and receiver side is measured. With a minimum execution time of 16.4 µs and a maximum of 57.2 µs the CBS processing of a class A stream results in a total CPU utilisation of 26.3 %. The inter-arrival time at the application

TABLE I
Memory consumption of the modules required for AVB

Module	Memory Consumption [kB]	%
Talker	4.7	2.5
Credit Based Shaper	55.8	29.0
AVB	62.2	32.5
AVB API	8.8	8.8
AVB Timer	2.0	2.0
MRP	41.8	21.8
MMRP	4.9	2.5
MVRP	4.8	2.5
SRP	7.1	3.7
Total	192.1	100.0

layer of class A frames (see Fig. 5) shows a slight jitter of $\pm 5\,\mu s$ which is caused by the send and receive routines. Since the bandwidth is calculated correctly and the timer which calls the send routine precisely triggers every $125\,\mu s$, this jitter is within an acceptable range for a CBS software implementation. The jitter is by magnitudes below the jitter imposed by concurrent traffic [18].

V. Conclusion & Outlook

Future in-car communication infrastructures are expected to rely on real-time Ethernet. For the challenging timing-requirements of such Ethernet based backbones, specialised software stacks for mixed-critical applications are required, to allow strict temporal precision and deterministic transmission.

With this paper we show a concept for a time aware credit based shaper and contribute a low footprint microcontroller based communication architecture supporting synchronous time-triggered and asynchronous event-triggered traffic in parallel while using standard hardware components. Our approach joins IEEE 802.1 AVBs credit-based shaper with a scheduler that provides support for time-triggered traffic, allowing the integration of the upcoming IEEE 802.1Qbv standard.

Our prototype implementation using a system-on-chip design with an ARM9 CPU running at only $200\,MHz$ shows the feasibility of the concept. It uses a minimal system with a simple priority based scheduler and hardware resources comparable with those utilised in upcoming series cars. Without further optimisation the implementation of AVBs credit based shaper utilises approximately $27\,\%$ of the available computation time. Together with the stream reservation protocol the stacks fingerprint is below $200\,kB$.

The Evaluation of the stack reveals a jitter of approximately $10\,\mu s$ measured in the reception routine of the receiver. This is the absolute jitter when using the presented implementation as sending and receiving device. As in average the inter-arrival time is $125\,\mu s$, the stack is in compliance with the reserved bandwidth contingents.

In future work we will improve the performance of the implementation. Further, we will analyse how specialised Ethernet hardware can support the traffic shaping to reduce CPU utilisation and software complexity.

Acknowledgements

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